Cost and Investment Implications of 3D NAND

Report No. FI-NFL-3DC-0514
Contents

CONTENTS .......................................................................................................................................... III
LIST OF FIGURES .................................................................................................................................. V
LIST OF TABLES .................................................................................................................................. IX
EXECUTIVE SUMMARY .......................................................................................................................... 1
INTRODUCTION ..................................................................................................................................... 3
THE PATH TO 3D .................................................................................................................................... 4
NAND Flash Technology Evolution ........................................................................................................ 4
3D NAND Flash Memory Cell .................................................................................................................. 6
Implementation of Floating Gate Cells into 3D NAND Flash Arrays ...................................................... 6
Floating Gate Memory Cell Scaling Challenges .................................................................................. 8
Charge Trapping Memory Cell Development and Remaining Reliability Issues ............................... 16
Optimization of Charge Trapping Memory Cell for the Application in 3D Arrays ............................... 19
2D AND 3D NAND PROCESS FLOW ................................................................................................... 25
Technology Overview and Process Challenges ................................................................................... 25
3D CONCEPTS .................................................................................................................................... 35
Overview .............................................................................................................................................. 35
CMOS formation .................................................................................................................................. 36
Conventional CMOS Adjacent to Memory Array .................................................................................. 36
CMOS Placement Below Memory Array .............................................................................................. 37
3D Memory Array Formation ................................................................................................................ 40
Toshiba p-BiCS .................................................................................................................................... 40
Samsung TCAT .................................................................................................................................... 49
3D Floating Gate .................................................................................................................................. 57
BEOL for 3D Concepts .......................................................................................................................... 62
Fundamental Limitation in 3D NAND Fabrication .............................................................................. 64
2D AND 3D NAND PROCESS COMPARISON ....................................................................................... 65
Process Complexity Comparison .......................................................................................................... 65
COST AND INVESTMENT IMPLICATIONS OF 3D NAND ....................................................................... 76
Greenfield Fab ..................................................................................................................................... 76
Fab Investment ...................................................................................................................................... 76
Equipment Footprint .............................................................................................................................. 81
Wafer RPT and Cycle Time .................................................................................................................... 83
Wafer Costs .......................................................................................................................................... 85
Sensitivity Analysis ............................................................................................................................... 87
Figure 30. BEOL stack after C2, metal 2 (M2), CL, and metal last (ML) generation and polyimide deposition and opening showing the nomenclature used.

Figure 31. Overview of the 3D NAND concept chapter and the 3D construction kit.

Figure 32. CMOS fabrication – STI finalization.

Figure 33. CMOS part - contact oxide deposition and polish after the implant steps and silicidation.

Figure 34. CMOS finalization – contact polish.

Figure 35. M0 formation right on top of the CMOS devices in case of CMOS below array.

Figure 36. CMOS below array with two finalized metal layers.

Figure 37. CMOS below array – final stage with transition contacts to connect the logic and artificial bulk to either use as connection layer (TCAT/3D-FG) or pipe formation layer (p-BiCS).

Figure 38. Overview of the initial proposal of the BiCS concept.

Figure 39. Structure of the p-BiCS concept.

Figure 40. Formation of the pipe structure to connect two associated memory cell chains.

Figure 41. Vertical etch of the channel holes to later place the charge trap stack and the memory string channel.

Figure 42. Formation of charge trap stack and channel with Macaroni structure and core filler.

Figure 43. Separation of control gates by vertical cut etch and subsequent fill with sacrificial nitride.

Figure 44. Select gate channel formation by hole etch stopping on memory string channel poly.

Figure 45. Separation of select gate planes by cut etch and removal of the memory cut etch sacrificial fill to allow silicidation of all gate planes.

Figure 46. a) Initial etch step to form the stair case gate connection structure, b) structure after one resist trim and cycle with two levels formed into the oxide, the periphery is etched accordingly to open the space for contacts to the CMOS part.

Figure 47. Finalization of the stair case etch by deposition of a nitride etch stop layer and oxide fill of the deep remaining trenches.

Figure 48. Contact formation to the stair case to provide electrical connection to the gate planes and CMOS part.

Figure 49. Intermediate structure with contacts to control gates, select gates and first metal layer M0 on top.

Figure 50. Schematic overview of the fundamental structure of the TCAT concept.

Figure 51. Schematic overview of the fundamental structure of the TCAT concept used in our proposal and the Samsung reference for V-NAND.

Figure 52. Structure after poly layer removal in the array area and multilayer stack deposition.

Figure 53. TCAT structure after channel hole formation and channel deposition with core filler.

Figure 54. TCAT - staircase formation status after 2nd etch cycle– 1st etch+1st strip+ 2nd etch.

Figure 55. TCAT structure after staircase etch finalization and oxide fill.

Figure 56. Intermediate structure with contacts to control gates, select gates and first metal layer M0 on top.

Figure 57. Intermediate TCAT structure with polished staircase fill oxide, etch gate cut and removed sacrificial nitride, the charge trap stack is already done with oxidized channel poly as tunnel oxide and deposited nitride and top oxide.

Figure 58. Finalization of the memory cells by deposition of the gate stack and recess etch, the electrical connection of the lower end of the string is solved by a junction implant through the gate cut creating a rectangular channel select device.

Figure 59. The 3D structure after the sourceline implant and subsequent silizidation to reduce the resistance, finally the gate cut is filled with oxide and polished.

Figure 60. The tungsten gate planes and the CMOS devices are contacted in the staircase structure by contacts with a huge height difference.
Figure 61. TCAT structure after M0 formation, the channel holes are separately contacted within the M0 processing

Figure 62. Comparison of the charge trap layer arrangement in (a) BiCS and (b) TCAT [28] and (c) SMarT [16]

Figure 63. a) Overview of the proposed 3D floating gate approach, showing 4 FG cells per string and the respective select devices, b) publication by SK Hynix and their proposal for a 3D FG structure with extended sidewall control gate –ESCG [29]

Figure 64. Initial state of the 3D floating gate NAND fabrication after the multilayer deposition, etched channel holes and FG cavity formation by anisotropic wet nitride recess etch

Figure 65. Vert. FG structure with finalized floating gates by poly deposition and wet etch for separation, subsequently the tunneling oxide is formed by thermal oxidation and the channel is formed by poly and core fill deposition

Figure 66. Vert. FG structure after staircase formation and subsequent oxide deposition to fill the resulting trenches

Figure 67. Vert. FG structure after sacrificial nitride removal to open the cavities for ILD deposition and control gate formation

Figure 68. Vert. FG structure with finalized control gates and IPD after metal deposition and subsequent wet recess for gate separation

Figure 69. Vert. FG structure with fabricated contacts to control gate planes and CMOS devices, furthermore sourceline silicidation is depicted by the purple circles

Figure 70. Vert. FG structure with formed connections to realize reliable upper select devices

Figure 71. Vert. FG structure after M0 formation which includes the connection to the vertical pipe channels on top of the contacts

Figure 72. BEOL stack after M1 polish including the finalized M1 and C1 on top of M0

Figure 73. BEOL stack after M2 oxide polish including the finalized M2 and C2 on top of M1

Figure 74. Final BEOL stack after Polyimid deposition and opening showing the used nomenclature in our process proposals

Figure 75. Final sequence of memory device gate fabrication in the 3D NAND approaches with recess etch, gate deposition and final wet etch gate separation, the formulas show the link between thickness of the horizontal layer and the gate cut dimension

Figure 76. Overview of the key contributors for 16nm NAND process complexity compared to 3D NAND

Figure 77. Process Complexity Drivers – 32L 3D NAND

Figure 78. Number of process steps by process group – 32L 3D NAND

Figure 79. Process Complexity Drivers – 64L 3D NAND

Figure 80. Number of process steps by process group – 64L 3D NAND

Figure 81. Lithography Layers by Technology

Figure 82. Main Thin Film Layers by Technology

Figure 83. Main Etch Layers by Technology

Figure 84. Main Clean Layers by Technology

Figure 85. 3D NAND Tool Commonality with 2D NAND

Figure 86. 2D NAND Tool Re-use in 3D NAND

Figure 87. Fab Investment by Technology

Figure 88. Number of Equipment

Figure 89. Equipment Investment Breakdown by Technology

Figure 90. Equipment Investment Breakdown by Process Module

Figure 91. Equipment Investment Breakdown by Process Module

Figure 92. Fab Investment by Tool Class

Figure 93. Equipment Footprint for 100kwpm Capacity
Figure 94. Equipment Footprint Breakdown by Process Module for 100k wpm Capacity ........... 82
Figure 95. Wafer Raw Processing Time Breakdown by Process Module ................................. 83
Figure 96. Wafer Processing Cycle Time by Technology .......................................................... 84
Figure 97. Front End Wafer Cost by Technology ................................................................. 86
Figure 98. Front End Wafer Cost Breakdown ........................................................................ 86
Figure 99. Fab Investment Sensitivity Analysis ....................................................................... 88
Figure 100. Equipment Footprint Breakdown for Given Area by Process Module for 32 Layer 3D NAND ................................................................................................................................................... 89
Figure 101. Impact on Wafer Capacity of Conversion from 2D NAND to 3D NAND .............. 90
Figure 102. Invest/De-invest for Conversion from 2D NAND to 3D NAND ............................. 91
Figure 103. Breakdown of Tool De-invest .................................................................................. 91
Figure 104. Incremental Invest by Technology for Conversion from 2D NAND to 3D NAND ................................................................. 92
Figure 105. % Increase in Incremental Invest by Technology for Conversion from 2D NAND to 3D NAND ............................................................................................................................................. 93
Figure 106. % Increase in No. of Tools by Technology for Conversion from 2D NAND to 3D NAND ................................................................................................................................................... 93
Figure 107. De-invest by Technology for Conversion from 2D NAND to 3D NAND .................. 94
Figure 108. % Decrease in No. of Tools (De-invest) by Technology for Conversion from 2D NAND to 3D NAND ................................................................................................................................................... 94
Figure 109. % Decrease in De-invest by Technology for Conversion from 2D NAND to 3D NAND ................................................................................................................................................... 95
Figure 110. Impact on Wafer Capacity of Conversion from 32L to 64L 3D NAND ............... 97
Figure 111. Investment/De-investment for Conversion from 32L to 64L 3D NAND .................. 98
Figure 112. Incremental Investment by Technology for Conversion from 32L to 64L 3D NAND ................................................................. 99
Figure 113. % Increase in Incremental Investment by Technology for Conversion from 32L to 64L 3D NAND ................................................................................................................................................... 99
Figure 114. % Increase in No. of Tools by Technology for Conversion from 32L to 64L 3D NAND100
Figure 115. De-invest by Technology for Conversion from 32L to 64L 3D NAND .................. 100
Figure 116. Wafer Raw Processing Time Breakdown by Process Module ............................. 102
Figure 117. Wafer Processing Cycle Time by Technology ........................................................ 103
Figure 118. Front End Wafer Cost by Technology ................................................................. 104
Figure 119. Front End Wafer Cost Breakdown ........................................................................ 105
List of Tables

Table 1. Comparison of the characteristic electrical parameters of p-BiCS and TCAT .......................24
Table 2. Comparison of the process complexity for 193 nm immersion litho vs. SADP and SAQP 33
Table 3. TCAT vs.SMaRT - Key Process Steps Comparison .................................................................56
Table 4. Fab Investment ........................................................................................................................81
Table 5. Equipment Footprint incl. support for 100k wpm Capacity ......................................................83
Table 6. Raw Processing Time/Cycle Time .........................................................................................85
Table 7. Front End Wafer Cost – 32L 3D NAND ................................................................................87
Table 8. Sensitivity Analysis – Total Fab Invest per 100k wpm ...........................................................88
Table 9. Conversion Costs from 100k wpm 16nm 2D NAND Fab ....................................................96
Table 10. Conversion Costs for 32 Layer to 64 Layer Migration .......................................................101
Table 11. Raw Processing Time/Cycle Time .....................................................................................103
Table 12. Front End Wafer Cost – 64L 3D NAND .............................................................................105
Table 13. Relative Comparison of 2D NAND and 3D NAND.............................................................106
Introduction

The NAND flash industry is on the cusp of a technology inflection point. 2D NAND is reaching its scaling limits with 3D NAND its anointed successor.

In the 2D NAND era, the underlying process technology (with a few exceptions) is essentially the same amongst all the NAND flash manufacturers.

However, in the 3D NAND era, all the NAND flash manufacturers are developing different 3D NAND concepts with variations in the process implementation. The different processes will impact the investment and manufacturing cost for each of the 3D NAND technologies.

This report provides a detailed analysis of the fab and manufacturing implications of 3D floating gate and charge trap NAND concepts from Samsung, Toshiba, SK Hynix and Intel-Micron versus 16nm 2D NAND. The analysis is based on a bottoms-up process flow analysis for each 3D NAND technology and 16nm 2D NAND.

Some of the questions addressed in this report include:

- What are the main drivers of the process complexity for 2D NAND and 3D NAND?
- What is the tool commonality between 3D NAND and 2D NAND?
- What is the cost impact of moving the CMOS under the array in 3D NAND?
- How much does it cost to build a Greenfield 3D NAND fab and how does it compare to a 2D NAND fab? What is the equipment footprint required and the breakdown of the investment by process modules?
- What is the front end manufacturing cost of a 3D NAND wafer compared to a 2D NAND wafer?
- What is the investment required to convert an existing 2D NAND fab to 3D NAND? What is the impact on the fab cycle time and manufacturing capacity?
- What is the incremental investment required to transition a 32 layer 3D NAND fab to 64 layers? What is the impact on fab cycle time and manufacturing capacity?
3D NAND Flash Memory Cell

The most important question with regard to the introduction of 3D NAND flash technologies is what is the most promising memory cell concept? The candidates are the floating gate (FG) and the charge trapping (CT) cell concepts. This single question can be elucidated into two questions, highlighting the most critical issues of the FG and CT cell concepts with regard to their implementation in 3D NAND strings.

- FG-Question 1: How can the very complex FG cell structure possibly be implemented into a 3D NAND array and benefit from the extensive 2D FG NAND experience?
- CT-Question 2: How can a CT cell work reliably in a 3D NAND array when it could never do so in 2D NAND?

These two questions will be answered in this introduction section which is focused on the implementation of FG and CT cells into 3D NAND strings.

Implementation of Floating Gate Cells into 3D NAND Flash Arrays

In the past, floating gate memory cells were used due to its reliable operation on the basis of a long experience over many technology generations.

One very important aspect of the floating gate cell reliability is the way these memory cells are programmed and erased. It is essential that the electrons which are moved during program and erase are solely transferred through the tunnel oxide (TOX) [1]. Every onset of electron transfer through the inter poly dielectric (IPD) will cause even higher tunnel currents flowing through the whole floating gate stack at higher programming levels and will strongly damage and finally destroy the floating gate cells affected.

The concentration of the tunnel currents to TOX requires a concentration of the voltage drop and therefore the electric field to this tunnel dielectric. This field concentration is an essential aspect of floating gate cells with a conducting FG due to an included capacitive voltage divider which cannot be realized in charge trapping cells. It is obtained by a floating gate cell design where the control gate (CG) to floating gate (FG) coupling area and therefore the CG-FG capacitance (C_{CG}) is sufficiently larger than the TOX coupling area and therefore the FG to cell channel capacitance (C_{TOX}) as depicted in Figure 2 (a) and (b).
3D concepts

Overview

The fabrication of the 3D-NAND concepts into the product is very similar. Since the memory array formation is separated from the logic, the CMOS periphery is quite comparable between the concepts. As shown in Figure 31, we offer two concepts of the CMOS integration. On the one hand, we analyzed the conventional CMOS formation besides the memory array. On the other hand, the array saving concept of shifting the CMOS below the array is considered. The area saving capabilities are analyzed in our report *How 3D NAND stacks up*.

![Diagram of 3D NAND concepts](image)

Figure 31. Overview of the 3D NAND concept chapter and the 3D construction kit

Next we introduce the three published concepts of the largest NAND manufacturers, namely, Toshiba p-BiCS, Samsung’s TCAT and the 3D floating gate approach of SK Hynix. The 3D NAND construction kit is finalized by the backend of line metallization package, which can be assumed comparable for all concepts.
The die is finalized with the last metal layer and polyimide coating. With the last etch the polyimide is opened called in our case TV (Figure 74).

Figure 74. Final BEOL stack after Polyimid deposition and opening showing the used nomenclature in our process proposals
xxxxx has two contributions which leads to a higher process complexity compared to the competing solutions. Firstly, more process steps are required to xxxxx and xxxxx. Secondly, a xxxxx independent of the xxxxx formation creates an additional overhead of approximately xx% higher process complexity. This is the largest contributor shown in Figure 77 driving the huge gap in process complexity. If both the xxxxx and xxxxx devices require a xxxxx formation, the process complexity for all the concepts will be similar and any differences will be due to the xxxxx formation.

The contribution of the 3D memory array formation to the total process complexity is xxxxx. A relatively large part is driven by the xxxxx, which is needed to xxxxx. This process sequence is highly dependent on xxxxx. For a 32 layer stack, this comes out to about xx% of the total process complexity in the xxxxx.
On the other hand, there is a shift from xxxx to more xxxx litho steps. This difference can be explained by a different need of xxxx steps during the fabrication process in case of the 3D NAND concepts.

Next, we give a closer look to the different deposition tools used in our POR proposals in Figure 82. Since the 3D NAND concepts are heavily reliant on deposition, the change for the different deposition techniques is dramatically higher compared to the previously reviewed lithography steps. In the case of xxxx, the number of process steps is xxxx for xxxx. This difference is caused by the fact that the xxxx are already formed during the multilayer deposition. The other concepts use xxxx layer as sacrificial material for the xxxx formation. Hence, the xxxx CVD tool utilization is tremendously higher compared to 16nm NAND.

The xxxx of the xxxx dictates the need for ALD deposition at the key steps. In case of 16nm NAND, we only assume xxxx the ALD steps for the xxxx. The 3D NAND concepts need ALD for the xxxx and additionally to form xxxx, which are finally separated by xxxx.
Although the number of xxxxx layers increases in 3D NAND, xxxxx as a proportion of the total equipment investment declines from xx% in 16nm NAND to xx%, xx% and xx% for p-BiCS, TCAT/SMArT and vertical FG respectively due to the xxxxx in 3D NAND.

Figure 89. Equipment Investment Breakdown by Technology

Figure 90. Equipment Investment Breakdown by Process Module
<table>
<thead>
<tr>
<th></th>
<th>p-BiCS 34L</th>
<th>TCAT/SMArT 36L</th>
<th>Vertical FG 36L</th>
<th>Vertical FG 36L CMOS below Array</th>
</tr>
</thead>
<tbody>
<tr>
<td>Capacity (k wpm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Incremental No. of Tools</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Incremental Equipment Invest ($ m)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>No. of Tools to De-invest</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Equipment De-invest ($ m)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Eqt Invest by Process Module</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Litho</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Implant</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Films</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Etch/Clean</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inspection</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Eqt De-Invest by Process Module</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Litho</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Implant</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Films</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Etch/Clean</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inspection</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>% Increase in No. of Tools by Process Module</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Litho</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Implant</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Films</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Etch/Clean</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inspection</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>% Decrease in No. of Tools De-Invested by Process Module</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Litho</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Implant</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Films</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Etch/Clean</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inspection</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Eqt Invest by Process Module % Change</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Litho</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Implant</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Films</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Etch/Clean</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inspection</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Eqt De-Invest by Process Module % Change</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Litho</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Implant</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Films</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Etch/Clean</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CMP</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Inspection</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 9. Conversion Costs from 100k wpm 16nm 2D NAND Fab
About the Authors

Florian Beug is Senior Technical Analyst for emerging memory technologies at Forward Insights. Florian’s career spans 10 years in the field of non-volatile flash memory. He was memory cell engineer responsible for 48nm floating gate and 36nm floating gate NAND flash development and the pre-development of 2xnm floating gate and charge trapping NAND flash memory at Qimonda AG. In addition, Florian was a member of the NAND flash pre-development team at Infineon focusing on 75nm, 63nm and 32nm TwinFlash/NROM charge trapping technologies and also worked on embedded floating gate flash cells of Infineon Technologies, STMicroelectronics and Philips Semiconductors/NXP.

He is the author or co-author of more than 30 publications in the field of reliability, degradation characterization, and modeling of future NVM technologies and holds patents in this subject area.

Florian holds a Masters degree in solid state physics and a Ph.D in Electrical Engineering both from the University of Hannover, Germany.

Thomas Melde is at GlobalFoundries Dresden. Previously, he was a Scientist at NaMLab GmbH responsible for charge trap flash device characterization, simulation, and reliability modelling. Thomas’ Ph.D. thesis focused on charge trap flash device development at the Flash pre-development team of Infineon/Qimonda, Dresden. He also worked as a research assistant at the Fraunhofer Institute, Division Design Automation, Dresden.

Thomas Melde received his diploma degree in electrical engineering at the Dresden University of Technology, Germany.

Stefan Slesazeck is a Senior Scientist at NaMLab GmbH, responsible for concept evaluation, electrical characterization and modelling for various memories, such as resistive memory and ferroelectric field effect transistor. Prior to NaMLab, he was a project leader for the pre-development of new memory concepts with Qimonda Dresden (Germany) focusing on concept evaluation for 1T – DRAM including floating body devices, cell concepts, access schemes for WL-driver and sense amplifier. As a device engineer at Infineon Technologies, Stefan focused on the module development of 3D DRAM access devices in 65nm and 46nm buried word line technology and pre-development of 3D DRAM access devices for FinFET and EUD.

Stefan received a Ph.D. in microelectronics from the Dresden University of Technology, Germany.
**Gregory Wong** is the Founder and Principal Analyst of Forward Insights. Greg has in-depth knowledge of the cost, performance and markets and applications of multi-bit per cell NOR, NROM and NAND flash memories, emerging memories and solid state drives. Greg previously held a number of management positions in strategic planning, business development and engineering at Hitachi, Siemens, ProMOS and Qimonda/Infineon. At Infineon/Qimonda, Greg was responsible for driving manufacturing efficiencies and investment planning for a DRAM fab in Taiwan. Subsequently, he became responsible for competitive intelligence and reverse engineering for flash memories focusing on flash memory vendors’ strategies, process technologies, design architectures, product performance, manufacturing capabilities and costs.

Greg earned his B.A.Sc. degree in Electrical Engineering from the University of Toronto, and his M.B.A. degree from the Richard Ivey School of Business in London, Ontario.
About Forward Insights

Forward Insights provides independent, insightful market research, consulting and information services focusing on semiconductor memories and solid state storage. The company offers unparalleled depth and understanding of the strategic, market and technical complexities of the semiconductor memory landscape.

Services

Forward Insights offers a unique and comprehensive strategic, financial, market and technical perspective on the semiconductor memory industry. The professional services offered include:

- Strategy Consulting
- Financial & Cost Analysis
- Market Forecasts
- Technology Analysis
- Competitive Analysis
- Surveys
- Training
- Custom projects

Contact

12 Appian Dr.
North York, Ontario
Canada  M2J 2P6
Tel.: +1-408-565-8207
E-mail: greg@forward-insights.com

Market and technical intelligence for semiconductor memories, emerging memory technologies and solid state drives.

www.forward-insights.com