



Phase Change Memory Enters a New Phase

Report No. FI-NVM-PCM-0708

By: Gregory Wong

July 2008

© 2008 Forward Insights. All Rights Reserved. Reproduction and distribution of this publication in any form in whole or in part without prior written permission is prohibited. The information contained herein has been obtained from sources believed to be reliable. Forward Insights does not guarantee the accuracy, validity, completeness or adequacy of such information. Forward Insights will not be liable for any damages or injuries arising from the use of such information including, without limitation, errors, omissions or inadequacies in the information contained herein or for the interpretation thereof. The opinions expressed herein are subject to change without notice.

Contents

CONTENTSIII

LIST OF FIGURES VI

LIST OF TABLESVIII

TERMINOLOGY.....1

EXECUTIVE SUMMARY2

MEMORY OVERVIEW3

 Introduction3

 The Memory Hierarchy.....3

 SRAM4

 Concept.....4

 Technology Evolution5

 DRAM7

 Concept.....7

 Technology Evolution8

 NOR Flash.....9

 Concept.....9

 Technology Evolution 11

 NROM..... 12

 Concept..... 12

 Technology Evolution 14

 NAND Flash 15

 Concept..... 15

 Technology Evolution 17

PHASE CHANGE MEMORY..... 20

 Introduction 20

 Phase Change Material 21

 Memory Cell Concept..... 23

 Basic Operation..... 23

 Memory Cell Variations..... 27

 Selection Device..... 29

 PCM Characteristics..... 30

 Set Time..... 30

 Reset Current 31

 Endurance 33

 Memory Comparison..... 33

Multi-level Cell PCM	36
Device Layout.....	39
PCM Reliability	43
PCM Cost Drivers	44
Die Size	44
Process Complexity.....	45
Technology Scaling	50
Scaling Parameters.....	50
Roadmaps	51
PCM DEVELOPMENT STATUS	55
PCM Development Status	55
ATMI, Inc.	56
BAE Systems.....	56
CAMELS	57
Elpida	57
Hynix Semiconductor	58
IBM.....	58
IMEC.....	58
ITRI	58
Macronix International.....	58
Nanochip	58
Numonyx (Intel/ST).....	59
NXP Semiconductors	59
Ovonyx.....	59
Qimonda AG.....	60
Renesas Technology.....	60
Samsung Electronics	60
STMicroelectronics.....	60
ULVAC	60
MARKET FORECAST	61
Applications.....	61
Market	64
REFERENCES	LXVIII
ABOUT THE AUTHOR.....	LXXII
ABOUT FORWARD INSIGHTS	LXXIII

Services lxxiii
Contact lxxiii

List of Figures

Figure 1. Memory Hierarchy4

Figure 2. SRAM Cell Layout5

Figure 3. 3D SRAM Technology.....6

Figure 4. DRAM Cell7

Figure 5. DRAM Cell Transistor Evolution.....8

Figure 6. DRAM Cell Capacitor Trend9

Figure 7. NOR Flash Cell.....10

Figure 8. NOR Architecture.....10

Figure 9. NOR Flash Cell.....10

Figure 10. NOR Flash Technology Evolution11

Figure 11. Drain Bias Margin12

Figure 12. NROM Cell Concept.....13

Figure 13. NROM Architecture13

Figure 14. NROM Cell13

Figure 15. NROM Technology Evolution14

Figure 16. Bit Disturb (“Second Bit Effect”)15

Figure 17. NAND Flash Cell Concept16

Figure 18. NAND Architecture16

Figure 19. NAND Cell String16

Figure 20. NAND Flash Technology Evolution17

Figure 21. NAND Flash Memory Gap Fill18

Figure 22. Electrons Stored on the Floating Gate.....18

Figure 23. Samsung 32Gb CTF Memory19

Figure 24. Timeline of Phase Change Memory20

Figure 25. Periodic Table.....22

Figure 26. GST Composition.....22

Figure 27. Basic PCM Cell Structure.....23

Figure 28. Set Operation24

Figure 29. Reset Operation25

Figure 30. Phase Change Memory I-V Curve.....26

Figure 31. Memory Array Operation.....26

Figure 32. μ Trench and Lance Structures.....27

Figure 33. Lance and pore structure28

Figure 34. Phase Change Bridge Memory.....28

Figure 35. MOS and BJT Selector29

Figure 36. Diode Selector.....30

Figure 37. Set Time Trend31

Figure 38. Dependence of Reset Current on Contact Area.....31

Figure 39. Reset Current Reduction with Ta₂O₅ Interfacial Layer.....32

Figure 40. Reset Current Trend.....32

Figure 41. PCM Endurance33

Figure 42. Read Access Time Comparison.....34

Figure 43. Write Throughput35

Figure 44. Program Performance Comparison36

Figure 45. MLC Write Approaches37

Figure 46. MLC Distribution37

Figure 47. Multi-level States as a Function of Pulse Tail38

Figure 48. 16-Level and 4-Level PCM.....38

Figure 49. Samsung Phase Change Memory Device Evolution39

Figure 50. Samsung 90nm 512Mb PRAM Layout.....40

Figure 51.	ST/Intel Phase Change Memory Device Evolution	40
Figure 52.	NOR Flash and PCM Architecture	41
Figure 53.	Intel 256Mb 130nm 28F256L18 StrataFlash Organization	42
Figure 54.	128Mb (256Mb MLC) PCM Organization	42
Figure 55.	Endurance as a function of Energy per Pulse	43
Figure 56.	PCM vs. NOR Flash	45
Figure 57.	Phase Change Memory Technology Evolution	46
Figure 58.	Samsung PRAM Cell Size Evolution	46
Figure 59.	SABEC Process.....	47
Figure 60.	PRAM Module.....	47
Figure 61.	180nm Process μ Trench PCM Process	48
Figure 62.	Phase Change Memory with μ Trench Cell.....	49
Figure 63.	Scaling Parameters.....	50
Figure 64.	PCM Scaling Challenges.....	51
Figure 65.	Memory Roadmaps.....	52
Figure 66.	Bit Size Trend	52
Figure 67.	Density Trend	53
Figure 68.	Areal Density Trend.....	54
Figure 69.	Embedded PCM Roadmap	54
Figure 70.	U.S. PCM Patents from 1990 to January 2007	55
Figure 71.	Radition-hard C-RAM.....	57
Figure 72.	Memory Device Characteristics - 2012	61
Figure 73.	PCM in the Memory System	62
Figure 74.	PCM as an Unified Memory	64
Figure 75.	PCM in the Memory Hierarchy.....	64
Figure 76.	\$/MB Forecast.....	65
Figure 77.	PCM NOR Replacement Rate.....	66
Figure 78.	Memory Revenue Forecast	67

List of Tables

Table 1. Memory Comparison34
Table 2. PCM Development Status56
Table 3. PCM DRAM Replacement Rate.....67