How 3D NAND Stacks Up

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Introduction

The NAND flash industry is at a technology inflection point. Planar floating gate NAND flash memory is facing fundamental scaling challenges with the upcoming 16nm node the last generation of planar technology. What's next?

Samsung's August 2013 announcement of the production of a 24-layer vertical string V-NAND shows the way forward. Vertical NAND or 3D NAND promises to continue increases in storage capacities and lower cost per bit necessary to enable emerging applications such as solid state drives and cold flash.

In the 2D planar era, the basic underlying floating gate technology (with a few exceptions) was essentially the same amongst all the NAND flash manufacturers. However in the 3D era, all NAND flash memory manufacturers are developing different 3D architectures.

How 3D NAND Stacks Up compares the 3D NAND alternatives and provides an independent view of the challenges, advantages and disadvantages of the various implementations and illuminates the 3D NAND status of the major industry players.

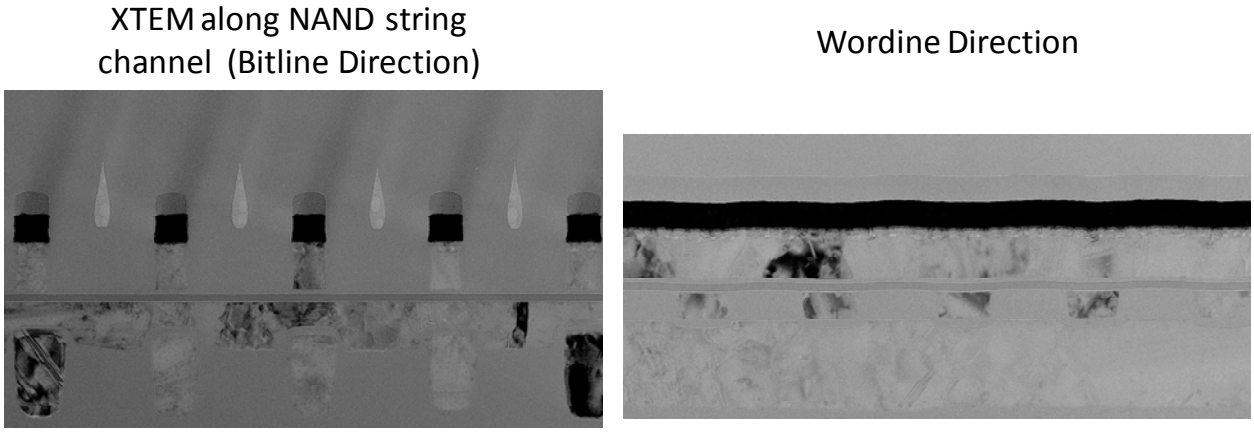

Figure 32. XTEMs dual gate SONOS devices [18]

The TEM cross section of Figure 32 illustrates the concept. It consists of a low thermal budget, inherently scalable, 3-D stackable, nitride based Flash solution with silicon TFT's having sub-50nm L and W devices built using standard CMOS fab tooling. Strings of up to 64 cells were fabricated with worst-case string currents in the 100's of nA's without special channel crystallization techniques and virtually zero read- and program-pass disturbs.

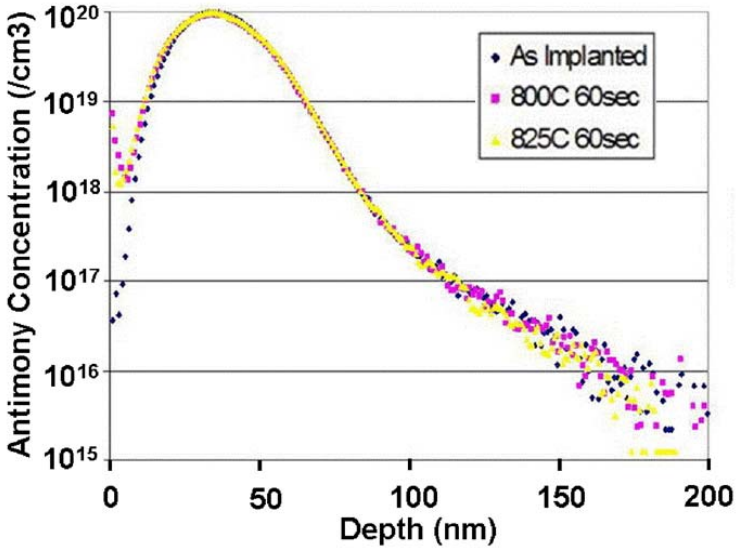

Figure 33. SIMS analysis of antimony-implanted LPCVD amorphous silicon, showing negligible diffusion [18]

Schiltron also addresses S/D formation. This is of even higher significance here since dopant diffusion in polycrystalline material is usually orders of magnitude greater than in monocrystalline silicon, a fact that would preclude the formation of ultra-short TFT's. In this research, however use is made of an extremely useful property of antimony where optimum activation in poly- and monocrystalline silicon occurs between 650°C and 800°C with no measurable diffusion. Figure 33 shows the SIMS analysis of antimony-implanted LPCVD amorphous silicon that subsequently underwent the illustrated thermal steps. This mimics the behaviour of the source and drain dopant

the following pages. The calculation leads to the smallest possible cell sizes and smallest feature size F which is required for the realization of the different 3D concepts.

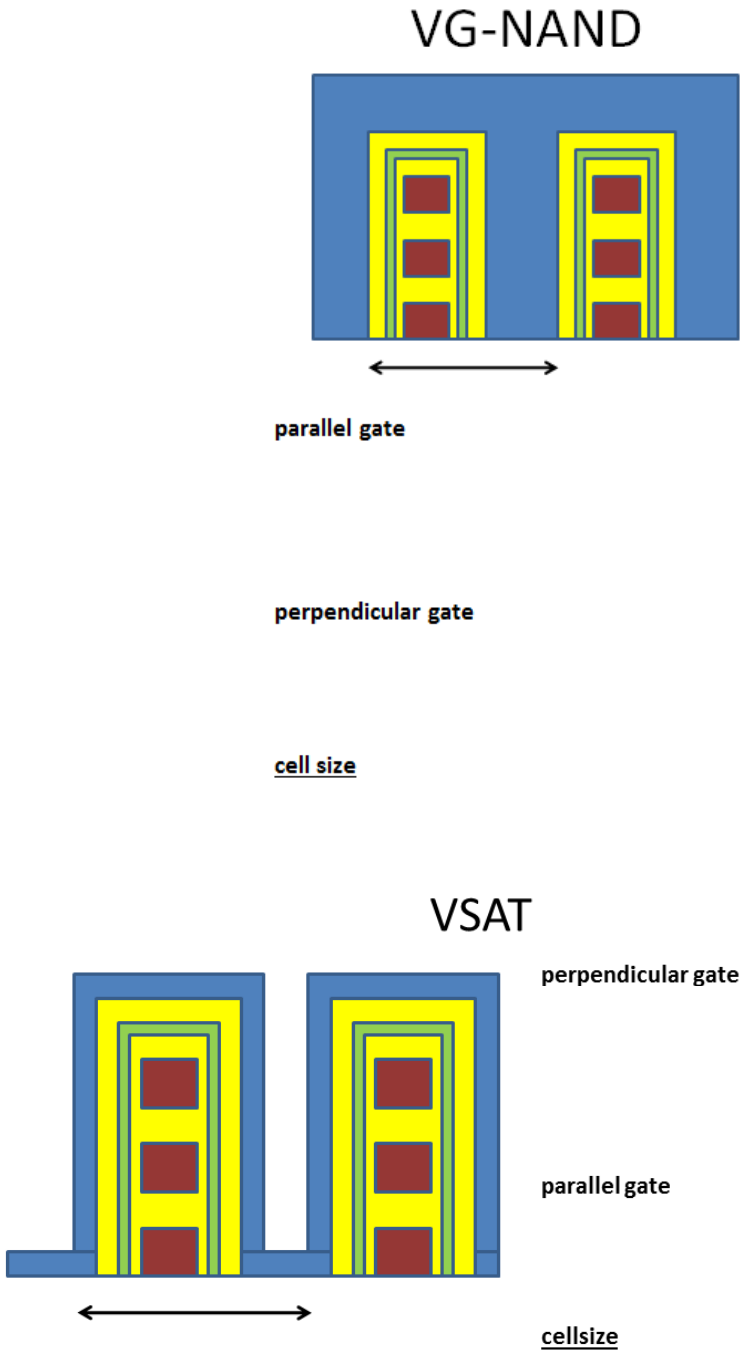

Figure 114. Minimum dimensions for VG-NAND and VSAT [NaMLab]

Performance

The specifications for 19nm TLC and MLC NAND flash is contrasted with our estimates for MLC V-NAND in Table 4. The performance is primarily impacted by the array architecture, periphery circuitry and layout optimizations as well as the use of charge-trap technology.

Specifications	MLC 19nm	TLC 19nm	V-NAND MLC 3xnm 24-layer
Density			
Page Size			
Block Size			
Voltage			
Operating I_{max}			
Program Time			
Block Erase (typ.)			
Access Time t_R			
Cycle Time			
Endurance (P/E cycles)			
Retention			
ECC bits/ KB			

Table 4 Specifications for NAND Flash vs. V-NAND [NAND datasheets, Forward Insights]

Most of the 3D concepts employ the charge trap stack for the memory element which benefits from

minimize the merge operation latency. For example, the block size of the 24-layer V-NAND is

In addition

Concept / Criterion	2D planar NAND	NOR	VG-NAND	p-BiCS	stacked cyl. FG	VSAT	TCAT / SMArT
Manufacturing complexity							
Performance							
Reliability							
Disturb							
Cost							
Cell size							
Stackability							
Scalability							
MLC capability							

Table 5. Comparison overview of the different concepts looking on all relevant aspects [Forward Insights, NaMLab]

Comments:

Manufacturing Complexity	yield, defect density, manufacturability
Performance	PGM/ERS speed, read speed
Reliability	endurance, retention
Disturb	PGM disturb/read disturb immunity
Cost (rel. cost/bit)	die size, process complexity, manufacturability, yield
Cell Size	physical cell size X/Y direction
Stackability	needed additional litho/process steps to stack an additional layer
Scalability	Ground rule scaling potential
MLC capability	is multi-bit storage really achievable

2D planar 20nm NAND flash is a proven technology that has the smallest cell size and MLC capability but faces further scaling limitations. All 3D NAND concepts suffer from

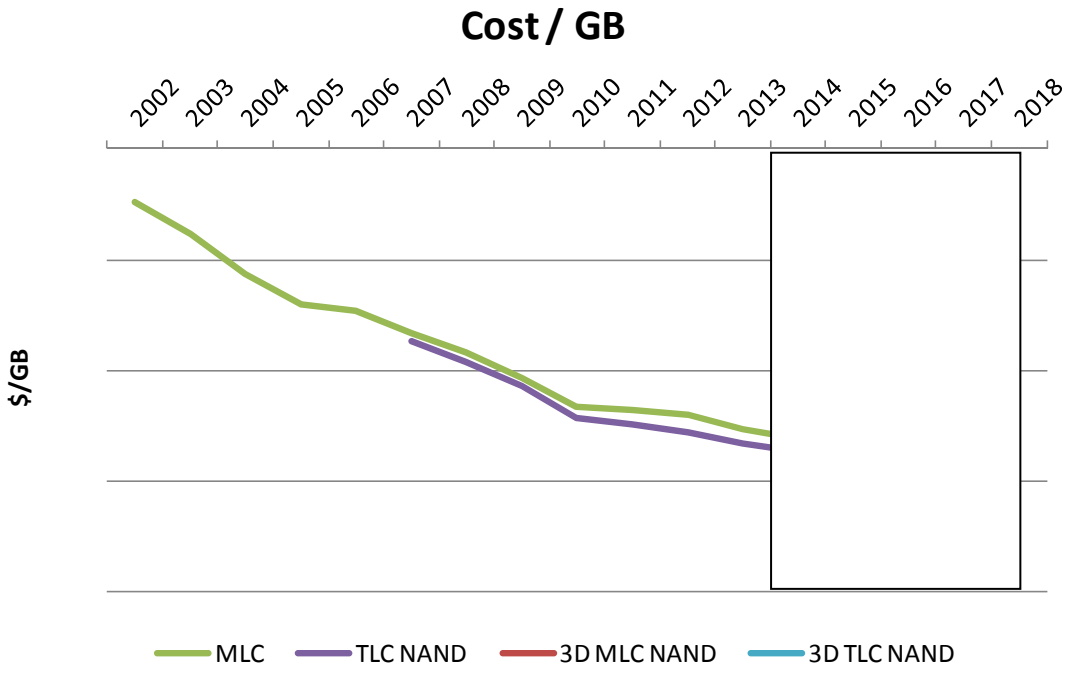

Figure 137. 2D and 3D NAND Cost Trend [Forward Insights]

About the Authors

Florian Beug is Senior Technical Analyst for emerging memory technologies at Forward Insights. Florian's career spans 10 years in the field of non-volatile flash memory. He was memory cell engineer responsible for 48nm floating gate and 36nm floating gate NAND flash development and the pre-development of 2xnm floating gate and charge trapping NAND flash memory at Qimonda AG. In addition, Florian was a member of the NAND flash pre-development team at Infineon focusing on 75nm, 63nm and 32nm TwinFlash/NROM charge trapping technologies and also worked on embedded floating gate flash cells of Infineon Technologies, STMicroelectronics and Philips Semiconductors/NXP.

He is the author or co-author of more than 30 publications in the field of reliability, degradation characterization, and modeling of future NVM technologies and holds patents in this subject area.

Florian holds a Masters degree in solid state physics and a Ph.D in Electrical Engineering both from the University of Hannover, Germany.

Thomas Melde is at GlobalFoundries Dresden. Previously, he was a Scientist at NaMLab GmbH responsible for charge trap flash device characterization, simulation, and reliability modelling. Thomas' Ph.D. thesis focused on charge trap flash device development at the Flash pre-development team of Infineon/Qimonda, Dresden. He also worked as a research assistant at the Fraunhofer Institute, Division Design Automation, Dresden.

Thomas Melde received his diploma degree in electrical engineering at the Dresden University of Technology, Germany.

Thomas Mikolajick is Head of the Chair for Nanoelectronic Materials and Scientific Director at NaMLab GmbH. He is also Head of the German Society for Materials Science (DGM) working group "materials for non-volatile memories" and coordinator of the Cool Silicon Cluster http://www.cool-silicon.de/. Previously, he was the Head of the Institute for Electronic- and Sensor Materials at TU Bergakademie Freiberg and lead new memory technologies and flash memory pre-development at Infineon Dresden.

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Stefan Slesazeck is a Senior Scientist at NaMLab GmbH, responsible for concept evaluation, electrical characterization and modelling for various memories, such as resistive memory and ferroelectric field effect transistor. Prior to NaMLab, he was a project leader for the pre-development of new memory concepts with Qimonda Dresden (Germany) focusing on concept evaluation for 1T – DRAM including floating body devices, cell concepts, access schemes for WL-driver and sense amplifier. As a device engineer at Infineon Technologies, Stefan focused on the module development of 3D DRAM access devices in 65nm and 46nm buried word line technology and pre-development of 3D DRAM access devices for FinFET and EUD.

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Gregory Wong is the Founder and Principal Analyst of Forward Insights. Greg has in-depth knowledge of the cost, performance and markets and applications of multi-bit per cell NOR, NROM and NAND flash memories, emerging memories and solid state drives. Greg previously held a number of management positions in strategic planning, business development and engineering at Hitachi, Siemens, ProMOS and Qimonda/Infineon. At Infineon/Qimonda, Greg was responsible competitive intelligence and reverse engineering for flash memories focusing on flash memory vendors' strategies, process technologies, design architectures, product performance, manufacturing capabilities and costs.

Greg earned his B.A.Sc. degree in Electrical Engineering from the University of Toronto, and his M.B.A. degree from the Richard Ivey School of Business in London, Ontario.

About NamLab

NaMLab (**Na**no-electronic **M**aterials **Lab**oratory)

The research at NaMLab focuses on materials for electronic devices and new device concepts. Among these are high-k materials for capacitors, transistors and other applications, novel switching devices including memristors, nanowire based electronics as well as materials for energy harvesting devices such as solar cells.

Future nano-electronic products require the development of new materials that are not currently available. NaMLab consequently focuses its research activities on materials and applications that show the potential to offer significant advantages over materials and products used today. In addition to investigating and characterizing new materials, NaMLab is undertaking research on the integration of these materials into semiconductor products with nano-scale dimensions.

NaMLab, originally founded as a research joint venture between Qimonda AG and the TU Dresden in July 2006, has its roots in the Corporate Research Department of Infineon AG and is now owned completely by the Technical University of Dresden. NaMLab receives basic financing from the Saxon Ministry of Science and Arts (SMWK). The company benefits from excellent working conditions in its office and clean room building opened in October 2007 and located within the TU Dresden campus.

Characterization:

- physical characterization (conductive AFM, SSRM, SEM)
- electrical device characterization;
    - 200mm/300mm wafer probe stations
    - 5K – 500K temperature range
    - Analytical measurements of memory cells (lifetime, switch time , storage and deletion windows, endurance and retention)
    - charge carrier mobility with Hall and split-C(U)
- optical characterization (FTIR ellipsometry, µRaman and photoluminescence)
- dielectric reliability (TDDB, BTI, SILC, TDDS, TSCIS)
- high-k material development
    - oxides: AlO, TiO, ZrO, HfO and mixtures
    - metals: Al, Pt, Au, TiN, Ti, Ru
    - methods: ALD, MBE, PVD, evaporation

Development:

- materials for emerging memories
- high-k stacks for capacitors and transistors
- development of new memory concepts
- charge trap device development
- development of explorative devices based on silicon nano wires

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About Forward Insights

Forward Insights provides independent, insightful market research, consulting and information services focusing on semiconductor memories and solid state storage. The company offers unparalleled depth and understanding of the strategic, market and technical complexities of the semiconductor memory landscape.

Services

Forward Insights offers a unique and comprehensive strategic, financial, market and technical perspective on the semiconductor memory industry. The professional services offered include:

- Strategy Consulting
- Financial & Cost Analysis
- Market Forecasts
- Technology Analysis
- Competitive Analysis
- Surveys
- Training
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